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semiconductor group
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6525 TRI-PORT INTERFACE

CONCEPT . . .

The 6525 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It combines two dedicated 8-bit I/O ports with a third 8-bit port programmable for either normal I/O operation or priority interrupt/handshaking control. Depending on the mode selected, the 6525 can provide 24 individually programmable I/O lines or 16 I/O lines, 2 handshake lines and 5 priority interrupt inputs.

FEATURES:

- 24 individually programmable I/O lines or 16 I/O lines, 2 handshake lines and 5 interrupt inputs.
- Priority or non-priority interrupts
- Automatic handshaking
- Completely static operation
- Two TTL Drive Capability
- 8 directly addressable registers
- 1 MHz, 2MHz and 3MHz operation

6525 Addressing

6525 REGISTERS/(Direct Addressing)

*000	R0	PRA – Port Register A
001	R1	PRB – Port Register B
010	R2	PRC – Port Register C
011	R3	DDRA – Data Direction Register A
100	R4	DDRB – Data Direction Register B
101	R5	DDRC – Data Direction Register C/Interrupt Mask Register
110	R6	CR – Control Register
111	R7	AIR – Active Interrupt Register

*NOTE: RS2, RS1, RS0 respectively

ORDER NUMBER:

MXS 6525

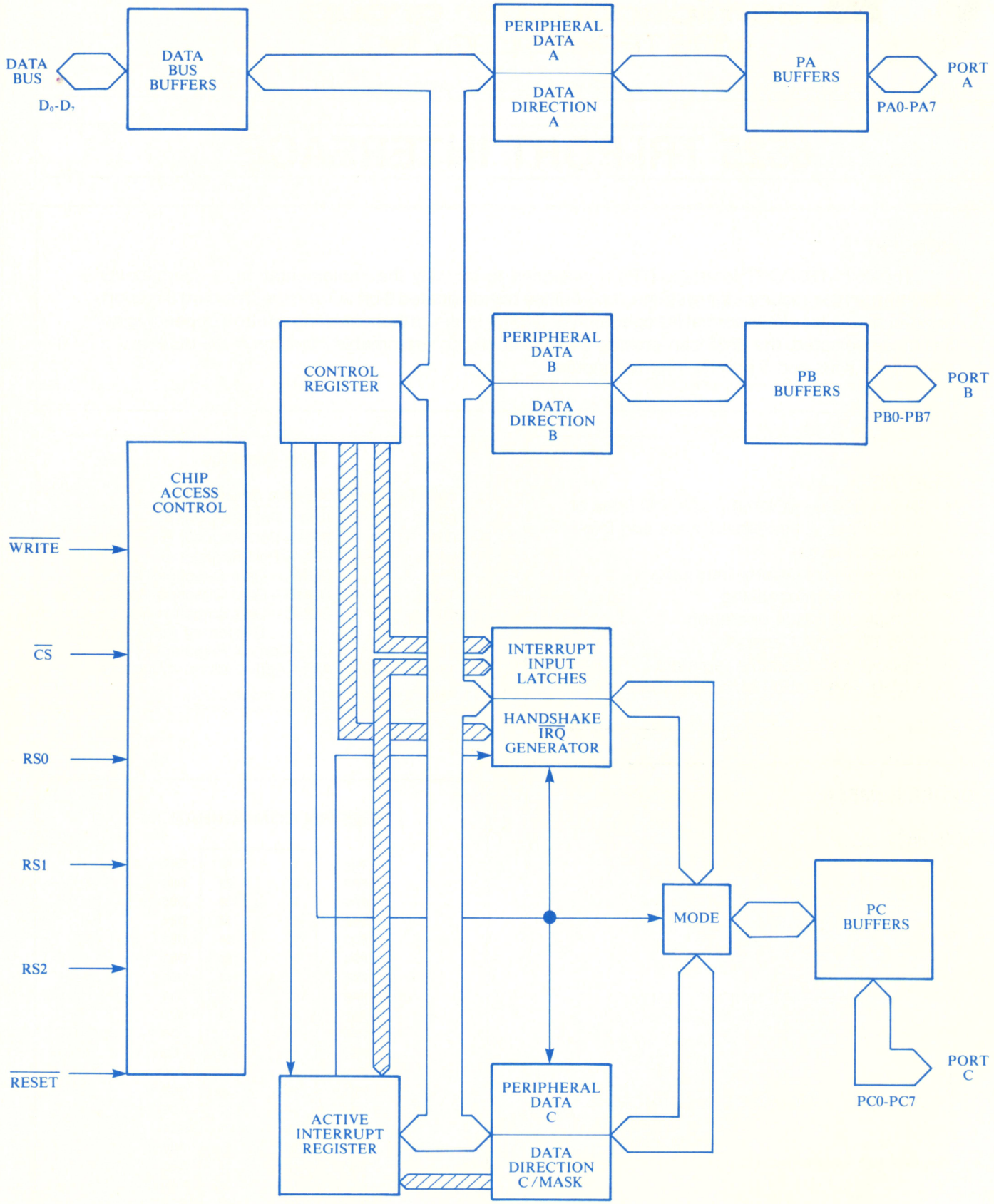
FREQUENCY RANGE
NO SUFFIX = 1 MHz
A = 2 MHz
B = 3 MHz

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

6525 PIN CONFIGURATION

V_{SS}	1	40	DB7
PA0	2	39	DB6
PA1	3	38	DB5
PA2	4	37	DB4
PA3	5	36	DB3
PA4	6	35	DB2
PA5	7	34	DB1
PA6	8	33	DB0
PA7	9	32	PC7
PB0	10	31	PC6
PB1	11	30	PC5
PB2	12	29	PC4
PB3	13	28	PC3
PB4	14	27	PC2
PB5	15	26	PC1
PB6	16	25	PC0
PB7	17	24	RS0
$\overline{CS}$	18	23	RS1
$\overline{WRITE}$	19	22	RS2
V_{DD}	20	21	$\overline{RST}$

6525 INTERNAL ARCHITECTURE



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	−0.3 to +7.0	V_{dc}
INPUT VOLTAGE	V_{in}	−0.3 to +7.0	V_{dc}
OPERATING TEMPERATURE RANGE	T_A	0 to +70	°C
STORAGE TEMPERATURE RANGE	T_{stg}	−55 to +150	°C

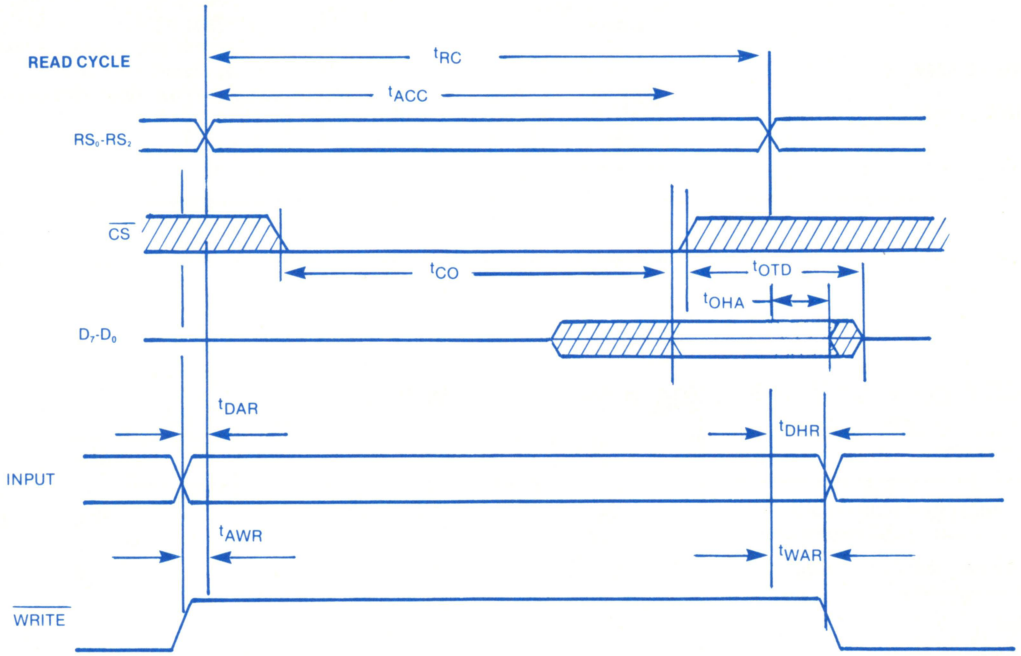
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

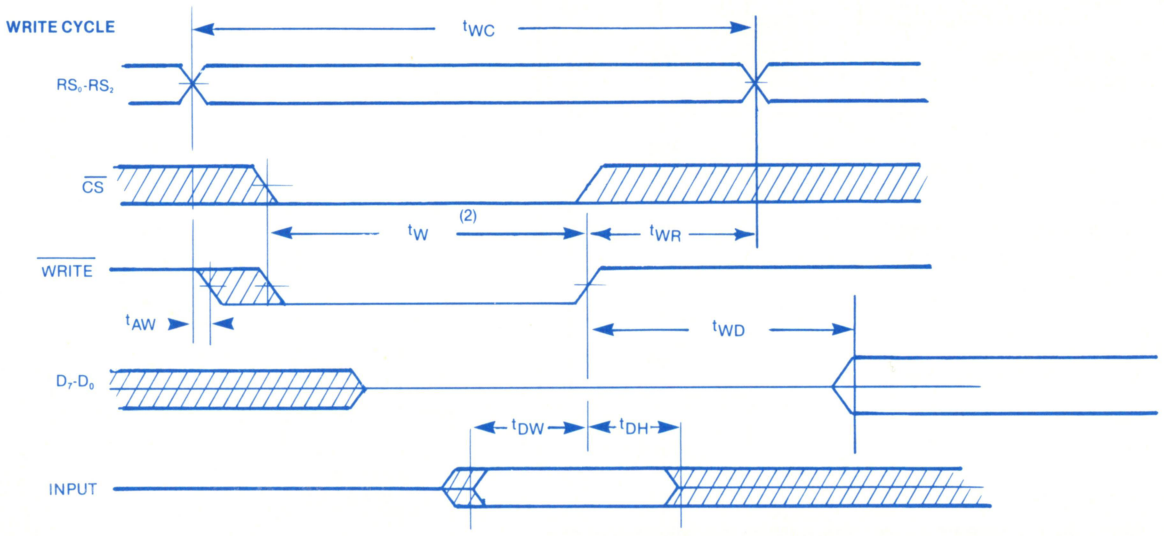
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	—	+.8	Vdc
Input Leakage Current V_{in} = 0 to 5.0 Vdc $\overline{WRITE}$ $\overline{RST}$, $\overline{CS}$, RS_0-RS_2	I_{IN}	—	±1.0	±2.5	μAdc
Three-State (Off State Input Current) (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) DØ-D7	I_{TSI}	—	±2.0	±10	μAdc
Output High Voltage (V_{CC} = min, Load = 200 μAdc)	V_{OH}	2.4	—	—	Vdc
Output Low Voltage (V_{CC} = min, Load = 3.2 mAdc)	V_{OL}	—	—	+0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc)	I_{OH}	−200	−1000	—	μAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	3.2	—	—	mAdc
Supply Current	I_{CC}	—	50	100	mA
Input Capacitance (V_{in} = O, T_A = 25°C, f = 1.0 MHz) DØ-D7, PAØ-PA7, PBØ-PB7, PCO-PC7, $\overline{WRITE}$ $\overline{RST}$, RS_0-RS_2, $\overline{CS}$	C_{in}	—	—	10	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	—	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE



WRITE CYCLE



READ CYCLE

Symbol	Parameter	1MHz MIN	1MHz MAX	2MHz MIN	2MHz MAX	3MHz MIN	3MHz MAX	UNITS
t_{RC}	Read Cycle Time	700		350		220		nS
t_{ACC}	Access time	450		200		130		nS
t_{CO}	Chip Select to Output Valid	450		200		130		nS
t_{OTD}	Chip Deselected to Output Off	0	100	0	100	0	100	nS
t_{OHA}	Output Hold From Address Change	50		50		50		nS
t_{DAR}	Peripheral Data Set-Up	90		80		60		nS
t_{DHR}	Peripheral Data Hold	0		0		0		nS
t_{AWR}	Write to Address Setup	0		0		0		nS
t_{WAR}	Write to Address Hold	0		0		0		nS

WRITE CYCLE

Symbol	Parameter	1MHz MIN	1MHz MAX	2MHz MIN	2MHz MAX	3MHz MIN	3MHz MAX	UNITS
t_{WC}	Write Cycle Time	700		350		220		nS
t_{AW}	Address to write set-up time	0		0		0		nS
t_{W}	Write Pulse Width	450		200		130		nS
t_{WR}	Write Release Time	250		150		90		nS
t_{DW}	Data to Write Overlap	150		75		75		nS
t_{DH}	Data Hold	50		50		50		nS
t_{WD}	Write to Peripheral Output	1000		500		330		nS

6525 Control Registers

CR	CB_1	CB_0	CA_1	CA_0	IE_4	IE_3	IP	MC
AIR				A_4	A_3	A_2	A_1	A_0
DDRC When MC = 1				M_4	M_3	M_2	M_1	M_0
PRC When MC = 1	CB	CA	$\overline{IRQ}$	I_4	I_3	I_2	I_1	I_0

CA, CB Functional Description

The CA, CB lines are outputs used in the same fashion as the CA_2 and CB_2 output of the 6520.

CA OUTPUT MODES

CA_1	CA_0	MODE	DESCRIPTION
0	0	"Handshake" on Read	CA is set high on an active transition of the I_3 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
0	1	Pulse Output	CA goes low for IMS after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	0	Manual Output	CA set low.
1	1	Manual Output	CA set high.

CB OUTPUT MODES

CB_1	CB_0	MODE	DESCRIPTION
0	0	"Handshake" on Write	CB is set low on microprocessor "Write B Data" operation and is set high by an active transition of the I_4 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
0	1	Pulse Output	CB goes low for IMS after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	0	Manual Output	CB set low.
1	1	Manual Output	CB set high.

INTERRUPT MASK REGISTER DESCRIPTION

When the Interrupt Mode is selected (MC = 1), the Data Direction Register for Port C (DDRC) is used to enable or disable a corresponding interrupt input. For example: If $M_0 = 0$ then I_0 is disabled and any I_0 interrupt latched in the interrupt latch register will not be transferred to the AIR and will not cause IRQ to go low. The interrupt latch can be cleared by writing a zero to the appropriate I bit in PRC.

PORT REGISTER C DESCRIPTION

Port Register C (PRC) can operate in two modes. The mode is controlled by bit MC in register CR. When MC = 0, PRC is a standard I/O port, operating identically to PRA & PRB. If MC = 1, then port register C is used for handshaking and priority interrupt input and output.

PRC When MC = 0:

PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0

PRC When MC = 1:

CB	CA	$\overline{IRQ}$	I_4	I_3	I_2	I_1	I_0

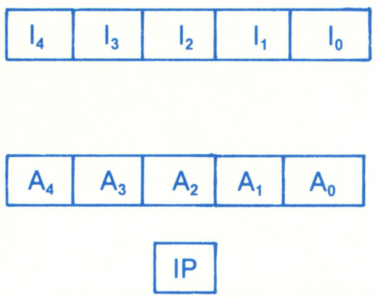
INTERRUPT EDGE CONTROL

Bits IE_4 and IE_3 in the control register (CR) are used to determine the active edge which will be recognized by the interrupt latch.

If IE_4 (IE_3) = 0 then I_4 (I_3) latch will be set on a negative transition of I_4 (I_3) input.

If IE_4 (IE_3) = 1 then I_4 (I_3) latch will be set on a positive transition of the I_4 (I_3) input.

All other interrupt latches (I_2, I_1, I_0) are set on a negative transition of the corresponding interrupt input.



Interrupt Latch Register
Clears on Read of AIR Using Following Equation

ILR ← ILR ⊕ AIR

Active Interrupt Register
Clears on Write to AIR

Interrupt Priority Select
IP = 0 No Priority
IP = 1 Interrupts Prioritized

FUNCTIONAL DESCRIPTION

1. IP = 0 No Priority

All interrupt information latched into interrupt latch register (ILR) is immediately transferred into active interrupt register (AIR) and $\overline{IRQ}$ is pulled low. Upon read of interrupt register the $\overline{IRQ}$ is reset high and the appropriate bit(s) of the interrupt latch register is cleared by exclusive OR-ing. The ILR with AIR (ILR⊕AIR). After the appropriate interrupt request has been serviced a Write to the AIR will clear it and initiate a new interrupt sequence if any interrupts were received during previous interrupt servicing. In this non-prioritized mode it is possible for two or more interrupts to occur simultaneously and be transferred to the AIR. If this occurs it is a software effort to recognize this and act accordingly.

2. IP = 1 *Interrupts Prioritized*

In this mode the Interrupt Inputs are prioritized in the following order $I_4 > I_3 > I_2 > I_1 > I_0$

In this mode only one bit of the AIR can be set at any one time. If an interrupt occurs it is latched into the interrupt latch register, the $\overline{IRQ}$ line is pulled low and the appropriate bit of the AIR is set. To understand fully the operation of the priority interrupts it is easiest to consider the following examples.

A. The first case is the simplest. A single interrupt occurs and the processor can service it completely before another interrupt request is received.

1. Interrupt 1_1 is received.
2. Bit I_1 is set high in Interrupt Latch Register.
3. $\overline{IRQ}$ is pulled low.
4. A_1 is set high.
5. Processor recognizes $\overline{IRQ}$ and reads AIR to determine which interrupt occurred.
6. Bit I_1 is reset and $\overline{IRQ}$ is reset to high.
7. Processor Services Interrupt and signals completion of Service routine by writing to AIR.
8. A_1 is reset low and interrupt sequence is complete.

B. The second case occurs when an interrupt has been received and a higher priority interrupt occurs. (See Note)

1. Interrupt I_1 is received.
2. Bit I_1 is set high on the Interrupt Latch Register.
3. $\overline{IRQ}$ is pulled low and A_1 is set high.
4. Processor recognizes $\overline{IRQ}$ and reads AIR to determine which interrupt occurred.
5. Bit I_1 is reset and $\overline{IRQ}$ is reset high.
6. Processor begins servicing I_1 interrupt and the I_2 interrupt is received.
7. A_2 is set, A_1 is reset low and $\overline{IRQ}$ is pulled low.
8. Processor has not yet completed servicing I_1 interrupt so this routine will be automatically stacked in 6500 stack queue when new $\overline{IRQ}$ for I_2 of interrupt is received.
9. Processor reads AIR to determine I_2 interrupt occurrence and bit I_2 of interrupt latch is reset.
10. Processor services I_2 interrupt, clears A_2 by writing AIR and returns from interrupt. Returning from interrupt causes 650X processor to resume servicing I_1 interrupt.
11. Upon clearing A_2 bit in AIR, the A_1 bit will not be restored to a one. Internal circuitry will prevent a lower priority interrupt from interrupting the resumed I_1.

C. The third case occurs when an interrupt has been received and a lower priority interrupt occurs.

1. Interrupt I_1 is received and latched.
2. $\overline{IRQ}$ is pulled low and A_1 is set high.
3. Processor recognizes $\overline{IRQ}$ and reads AIR to determine that I_1 interrupt occurred.
4. Processor logic servicing I_1 interrupt during which I_0 interrupt occurs and is latched.
5. Upon completion of I_1 interrupt routine the processor writes AIR to clear A_1 to signal 6525 that interrupt service is complete.
6. Latch I_0 interrupt is transferred to AIR and $\overline{IRQ}$ is pulled low to begin new interrupt sequence.

NOTE: It was indicated that the 6525 will maintain Priority Interrupt information from previously serviced interrupts.

This is achieved by the use of an Interrupt Stack. This stack is pushed whenever a read of AIR occurs and is pulled whenever a write to AIR occurs. It is therefore important not to perform any extraneous reads or writes to AIR since this will cause extra and unwanted stack operations to occur.

The only time a read of AIR should occur is to respond to an interrupt request.

The only time a write of AIR should occur is to signal the 6525 that the interrupt service is complete.